

What is claimed is:

✓ 1. A device, comprising:

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5 a delay lock loop circuit responsive to an input signal
to delay the input signal by a first period; and
a delay circuit coupled to the delay lock loop circuit
and responsive to the input signal, the delay circuit being
responsive to a control signal from the delay lock loop
circuit to delay the input signal by a second period.

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✓ 2. The device of claim 1, wherein the input signal
comprises complimentary input clock signals.

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✓ 3. The device of claim 2, wherein the first period and
the second period are substantially the same.

✓ 4. The device of claim 2 further comprising a first
input channel coupled to the delay lock loop circuit and a
second input channel coupled to the delay circuit.

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Sub B2 ✓ 5. The device of claim 1, wherein the delay lock loop
circuit further comprises:
at least one delay cell; and

a phase detector responsive to the input signal and responsive to an output signal from the at least one delay cell to produce a control signal.

5 6. The device of claim 1, wherein the delay circuit further comprises at least one delay cell responsive to the control signal from the delay lock loop circuit.

10 ✓ 7. The device of claim 1, further comprising; a latch circuit having a first input to receive an input data signal and a second input to receive one of an output from the delay circuit and an output from the delay lock loop circuit.

15 8. The device of claim 7, wherein the delay lock loop circuit comprises a center tap.

✓ 9. A device, comprising:
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20 a delay lock loop circuit responsive to a first input signal to delay the first input signal by a first period; and
B3 a delay circuit coupled to the delay lock loop circuit and responsive to a second input signal, the delay circuit being responsive to a control signal from the delay lock loop circuit to delay the second signal by a second period.

✓ 10. The device of claim 9 wherein the first signal and the second signal comprise complimentary clock signals.

5 ✓ 11. The device of claim 9 further comprising a latch circuit, the latch being responsive to one an output of the delay lock loop circuit and an output of the delay circuit.

10 ✓ 12. The device of claim 9 wherein the delay lock loop circuit comprises at least one delay cell.

15 ✓ 13. The device of claim 11, wherein the delay circuit further comprises at least one delay cell responsive to the control signal from the delay lock loop circuit.

✓ 14. A method, comprising:

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20 ✓ receiving a first signal and a second signal;
using a delay lock loop circuit to delay the first signal by a first period; and

✓ using a delay circuit to delay the second signal by a second period in response to a control signal from the delay lock loop circuit.

15. The method of claim 14, wherein the using the delay lock loop circuit comprises configuring the delay lock loop circuit with at least one delay cell.

5 ✓ 16. The method of claim 14 further comprising activating a latch circuit in response to one of an output from the delay lock loop circuit and an output from the delay circuit.

10 ✓ 17. The method of claim 14, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal.

15 ✓ 18. The method of claim 14, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal and the method further comprising activating a latch circuit on a rising edge of one of the first delayed clock signal and the second delayed clock signal.

20 ✓ 19. The method of claim 14, wherein the first period and the second period are substantially the same.

✓ 20. The method of claim 14, wherein the using the delay circuit further comprises configuring the delay circuit with

at least one delay cell and using the control signal to adjust
the at least one delay cell.